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# SRAM Bit Cell Designed With A Focus On Security In A 7T Configuration

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***Abstract* - Power analysis (PA) attacks have emerged as a serious threat to security systems since they allow for the extraction of confidential data. These attacks are carried out by analyzing the current that is consumed by the system's power supply. Embedded memories are an essential component of these systems. These memories are typically constructed using six-transistor (6T) static random-access memory (SRAM) cells at the time of implementation. Because of the connection between the current characteristics and the data that has been written, conventional SRAM cells are susceptible to attacks that include side-channel power analysis. The 7T SRAM cell that we have presented is intended to be more secure and resistant to assaults of this kind. it utilizes a two-phase write operation and has an additional transistor in comparison to the 6T SRAM version, the data that is stored is much less connected with the amount of power that is used during write operations. The proposed 7T SRAM cell, when constructed utilizing a 28 nm technology, demonstrates a write energy standard deviation between write '1' and '0' operations that is more than a thousand times lower than that of a conventional 6T SRAM as compared to the energy standard deviation. The recommended cell has a shorter write latency of 19% to 38% and a lower write energy of 39% to 53% when compared to current power analysis resistant SRAM cells. Additionally, the suggested cell has a lower write energy of 39% to 53%.**

***Keywords:*** **SRAM, 7T, Cells, Extraction, Power Analysis, Transisitor.**

## I. INTRODCUTION

Standard Random Access Memory (SRAM) continues to be an essential component for system-on-a-chips (SoCs). As battery-operated portable applications continue to become more prevalent, they are increasingly depending on the low-power feature of on-chip SRAMs. On the other hand, high-speed VLSI circuits encounter this problem as a significant obstacle since their primary objective is not to lower the amount of power that they use but rather to achieve excellent performance. On-chip SRAMs often include a substantial number of bits, Range from 16 to 256 or even more. This is because the complexity of systems that are designed to improve performance is expected to continue to increase.

The advancement of very large scale integration (VLSI) has made it possible for FINFET SRAM to come into existence. This game-changing technology offers a 7 nm transistor design to fulfill the requirements of an upgraded storage system. As a result of the three-dimensional gate design, the controlling dependencies on traditional drain and source terminals are reduced, which is the fundamental rationale for this innovative technology. Traditional transistor designs have a problem with the short channel effect; however, the modern FINFET design philosophy completely removes this problem that was previously present. For the reason that FINFETs do not possess a channel doping mechanism, they are able to circumvent a problem that is encountered by traditional MOSFETs, which is the alteration of arbitrary dopant. When compared to planer CMOS circuits, FINFET circuits have lower levels of supply voltage. This is there are fewer energy points and fewer sites for the product of delay and energy in FINFET circuits. The FINFET does this by enhancing the voltage stability. Memory storage systems such as serial random access memory (SRAM) are experiencing problems with maximum power consumption from the chip and high occupancy of cache memory in the chip area simultaneously.

The operation of a Fin FET may be carried out in two distinct ways: either as an independent gate or as a tied gate. Through the process of connecting the two gates together, a tied gate FinFET may be transformed into an ON/OFF switch. In an independent gate FinFET, one gate is responsible for controlling the threshold voltage of the device, while the other gate is in charge of switching. Using FinFETs that are operated with a multi-threshold voltage, which give superior read, write, and hold margins, is a great way to improve the stability of memory circuits. The MOSFET operates in the week-inversion area, which is also referred to as the sub-threshold zone. This occurs when the gate-to-source voltage is just below the threshold voltage of the device. Despite the fact that it is expected that a MOSFET would operate in its OFF state before the threshold voltage is reached, current may be conducted from the source to the drain even at voltages that are lower than the threshold value. Although it

is also known as sub-threshold conduction, the term "sub-threshold leakage" is the one that is most often used to describe this phenomenon seen in lower-tech nodes. A significant portion of leakage current is generated by it. Utilizing transistor stacking at the circuit abstraction level is an effective method for reducing leakage. The fine grain power gating strategy is employed at the circuit abstraction level, whereas the coarse grain power gating approach is applied at the architectural abstraction level. There are two types of low power approaches. The results of this research demonstrate that the power consumption of a 6T-SRAM cell as well as an array of multiple memory cells may be successfully decreased by using these strategies. Additionally, the 6T SRAM cell is used it has superior stability features and enables more compact packaging.

The scaling of devices raises a number of design challenges in the nanoscale design community [4]. When it comes to the design of SRAM cells, stability is the key focus. Operating conditions and the aspect ratio of the MOSFET both have an effect on the memory's capacity to maintain its stability. It is the purpose of stability to ensure that memory is operated accurately. The Static Noise Margin (SNM) measure indicates that the SRAM cell is an example of a stable device.For the purpose of deriving the SNM, the voltage transfer parameters of the SRAM cell are used. To alter the state of an SRAM, the SNM noise, which has the lowest voltage, is capable of doing so. While it is essential that SRAM permits new data to be written into it during the write phase, it is as essential that the value that is stored in it should not change when it is read. The total amount of power that is lost by SRAM is the sum of all of its power dissipation, regardless of whether it is static or dynamic.The SRAM makes use of dynamic power while it is operating in its typical read/write mode, and it makes use of standby power when it is operating in its standby mode at the same time. The major objective of this article is to investigate and construct a 6T SRAM cell by using a number of different CMOS technologies, with a particular emphasis on stability. For the purpose of this inquiry, PTM model cards are used to explore the performance characterization of the cell in a variety of modes. Additionally, it provides a wide range of process alternatives in model files that are accurate and compatible with one another. Cadence Virtuoso Analog Design Environment is the tools that we employ to fulfill all of our requirements for design and simulation.

## II. LITERATURE SURVEY

The team consisting of Hoang Anh Du Nguyen, Lei Xie, Mottaqiallah Taouil, Razvan Nane, Said Hamdioui, and Koen Bertels has chosen an outstanding scenario that is based on an in-memory model. The goal of this scenario is to increase communication and energy efficiency. To ease difficulties related to poor performance and energy consumption, the majority of the currently available communication architectures need just a small amount of memory. The term "Computational In Memory" refers to a storage reference that combines a variety of computationally essential solutions into design designs. Taking into account the evidence that is now available, this design suggests making use of the GPUs and CIMs that are already in existence to carry out data processing in massively parallel structures. This would result in improved energy and area performance.

It was Akshatha P. Inamdar, P. A. Divya, and H. V. Ravish Aradhya who were successful in achieving the design process parameters for CMOS technology modeling. To assure stability, leakage power analysis, and peak performance, the design cell only uses 8.54 percent less power on the data line while it is being read or written. In addition, the 9T design would reduce the amount of power that is used by typical 2-bit data lines, which would cause access times to be shortened. Real-time data transmission from the central processing unit (CPU) to memory is accomplished by cache memory, which is an essential component of the processor and memory unit. A subset of use cases has grown more dependent on memory scaling, which has become a key role to perform in a range of technologies connected to CMOS. It is possible that failures in both the functional and electrical aspects of memory might propose a new way of looking at memory analysis and modeling. There were many different design models that were researched and evaluated for reading and writing operation conditions, including verification and stability analysis. These models included memory cells with a capacity of 8 T and memory cells with a capacity of 6 T. When nanoscale technology for 45 nm employing CVD is taken into consideration, a few important parameters, together with its voltage and current characteristics, would be sufficient to generate a low-energy scenario and limit energy leakage. An integrated low power consumption research would suggest the expansion and its essential scenario to improve memory units with regard to storage density and low power consumption. This would be done to increase memory units. A design model for the current thesis presents performance characteristics and graphical assessments of the different models' design needs. The design model is based on 6_T, 7_T, 8_T, and 9_T cells. It may be possible to decide which cell will give the optimum real-time scenario by doing an analysis of the power consumption scenario and its impacts on latency and noise margins in static leakage values for current and voltages.

Memory or system on a chip (SoC) that devotes an ever-growing percentage of its surface area to memory may have its whole power budget dominated by standby leakage power. This is because memory consumes an increasing amount of total surface area. The scaling of the supply voltage (VDD) is an effective way for lowering the amount of power that is lost in the standby state of SRAM and cache. The sub-threshold leakage current (which is generated by DIBL) and the gate leakage are both decreased when the voltage is scaled down, in addition to the obvious power savings that result from switching to a lower voltage. Reduce VDD as much as is practically possible to maximize the savings that may be achieved from leaking power. On the other hand, data loss happens when the VDD is lowered with an excessive amount. Bitcell data is safeguarded up to a certain point by the data retention voltage (DRV), which is the minimum standby supply voltage. This value is baseline voltage inside-die device variance, sometimes referred to as mismatch, is the reason of the peculiar DRV distribution that is possessed by

every single cell that is included inside a memory array. Monte-Carlo (M-C) simulation is a well-known currently available method that may be used to ascertain the worst-case DRV for an SRAM array. This is accomplished by taking into consideration the array size as well as the statistical properties of the device variation. Having said that, it is possible that M-C simulations for large arrays that need extended tail runs (i.e., more than 6σ) might be very time-consuming. Fig. 1 is the histogram of a 5k-point M-C simulation, and it displays the DRV for SRAM bitcells that have a threshold voltage (VT) fluctuation that is regularly distributed throughout the die. It is not feasible to extrapolate small Monte-Carlo simulations by modeling the tail with a normal distribution because the DRV does not follow a normal distribution. This is because the DRV does not follow a normal distribution.

The Schmitt Trigger SRAM cell, which was proposed by Jaydeep P. Kulkarni et al. [15], outperforms the conventional 6T SRAM cell by 56% in terms of SNM, process variation tolerance, read failure probability, low voltage/power operation, and data retention capability at ultra low voltage. This is because the Schmitt Trigger SRAM cell has a built-in feedback mechanism. While running at a decreased voltage drop of 175 mV VDD, they discovered that the recommended memory bit cell outperformed the conventional 6T cell by 18% in terms of leakage reduction and by 50% in terms of read/write power consumption at iso-area and iso-read-failure probability. This was accomplished while the memory bit cell was operated at a reduced voltage drop. According to the results of their simulation investigation, the memory bit cell that was proposed is capable of storing data at a supply voltage of 150 millivolts. Using the memory bit cell that was described, functioning SRAM was demonstrated inside the 0.13µm CMOS technology at a voltage of 160 mV.

The read SNM limitation was eliminated by Naveen Verma and colleagues [16] with the implementation of an 8T bit-cell that included a buffered read configuration. Further, the peripheral footer circuitry is responsible for removing any bitline leakage that may have occurred. Additionally, the peripheral write drivers and storage-cell supply drivers of the authors collaborate to bring the cell supply voltage down while write operations are being performed. An excellent trade-off between area and offset is achieved as a consequence of the additional sense-amp redundancy that is provided. It was found that the 65 nm SRAM array was operational at 350 mV, and it was determined that data was correctly maintained at 300 mV respectively.

## III. EXISTING SYSTEM

To store sensitive information, a wide variety of applications, such as smart cards and mobile devices, depend on cryptographic devices. The use of these devices has significantly expanded over the course of the last several decades. These devices are vulnerable to a severe threat known as side channel analysis (SCA), which is a method of stealing private information by using data about the devices' physical activities. PA attacks are among the most effective SCA tactics because of the minimal complexity of the hardware and software that is required while using them. The purpose of an attack that makes use of PA is to divulge sensitive information by taking advantage of the correlation that exists between the data that has been processed and stored on the device and the instantaneous current that is consumed by its power source.

Embedded memory is a key component of many cryptographic systems, including smart cards and wireless networks that use cryptography techniques. Embedded memory stores instruction code and data, and it also dominates the size and power consumption of many very large scale integrated circuits (VLSI SoCs). Consequently, there is an extremely high level of significance in the research and development of protected memories. The 6T SRAM macrocell is the most prevalent implementation for embedded memory. This is it has a high density, operates in a durable manner, and performs very well. On the other hand, 6T SRAM arrays are famously susceptible to PA attacks their security protections are often ignored in favor of high density and performance enhancements.

Using redesigned SRAM bitcells, it has been proposed in earlier papers that the correlation between the data that is stored and the dynamic power consumption of a regular 6T SRAM array may be reduced. Both of these methods are built on the basis of a two-stage sequential writing process. The first step is to pre-charge the internal nodes of the SRAM cell (Q and QB) to a constant voltage. This is done to guarantee that the write operation does not have any impact on the data that has been stored in the past. To power-cut the supply during the extra pre-charge phase, the authors suggested carrying out the pre-charge operation using two additional PMOS transistors in addition to the 6T SRAM that was initially used. It was recommended by the authors of that a feedback-cut SRAM cell be used to reduce power loss that is caused by short circuits. This particular kind of cell makes use of two additional NMOS transistors to block the feedback of the SRAM cell. There is a reduction in static noise margins (SNMs), a discernible increase in latency, and an overall rise in power overheads as a result of these approaches; nonetheless, they are effective in reducing the correlation between the power consumption of the SRAM array and the data that is stored.

When we talk about side-channel attacks, we often assume that the attacker is acquainted with the architecture of the chip, which includes its memory organization, array peripherals, and internal clock pathways, and that he also has access to the connections that are used for the power supply of the system. In addition, it is anticipated that an adversary may control the system by feeding it input vectors, which could result in write operations being performed on certain rows in information storage. As a last point of discussion, it is often considered that the total current that is used by the memory macro peripherals and other chip components may be reduced to algorithmic noise with the utilization of adequate current traces. In particular, this is true in situations when the memory array is powered by a separate level of supply voltage.

The purpose of this study is to provide a novel design for static random access memory (SRAM) cells that consists of seven transistors and has a focus on security. It is PA resilient because the design makes use of a two-phased write operation, which significantly reduces the connection between the data that is written and stored in the memory and the amount of power that is used by the memory. The recommended 7T cell incorporates one transistor into the basic 6T SRAM architecture and makes use of one power gate transistor for each memory word. This is done to achieve the goal of standardizing the Q and QB voltages during the first stage of the write operation process. When compared to existing PA resilient memory systems, the recommended cell performs better in terms of energy dissipation (-39% to -53% lower), write latency (-19% to 38%), and read and hold SNMs (the highest).

## IV. PROPOSED SYSTEM

Devices that are based on cryptographic applications have lately emerged as an essential component in the process of storing and retrieving data that is becoming more sensitive. As a result, it takes advantage of the connection that exists between the instantaneous current that is used by power supply devices and information leakages, and it also has an impact on power analysis and side channel analysis. Two-phased write operations are used in the novel 7T SRAM cell design that is presented in this article. These actions significantly reduce the relationship between memory power consumption and the amount of data that is written and stored, which makes the architecture resistant to power analysis. When compared to the present 6T SRAM technology, which employs one power gate transistor for each memory, the 7T cell that is being suggested contains one additional transistor. It is our intention to construct a 7T SRAM bit cell using 22nm CMOS technology with the use of TANNER EDA Software for this project. In comparison to the existing 6T SRAM bit cell, it will be smaller, quicker, and less power leaking. Additionally, it will be capable of performing operations at both the single bit and 8-bit level.

### A. Cell Design Consideration

As a tradeoff, read latency, noise margin, and cell area are all factors that are taken into consideration while constructing cells for the system that has been presented. Initially, the tradeoffs are discussed in regard to two switch design parameters, Vss: b and N. After that, a quantitative assessment of these three challenges is carried out. The read cycle equivalent circuit of a proposed cell is shown in Figure 1.5 for our own viewing pleasure. A stack consisting of three nMOS transistors may be found along the path that read current takes. A cell access transistor has a width of Wa, a cell driver transistor has a width of Wd, and the switch Vss has a width of Wsw. There are three widths. A ratio of Wsw to Wd is the definition of the first crucial design parameter, which is denoted by the letter b. b is no longer reliant on technology-specific variables, the following considerations may be applied to any technology node that has such a description. Within a typical six-transistor cell, the value of Wd is normally set at 3Wa, but the value of b is nearly infinite. It is expected that the read current and the static noise margin will decrease after the finite-value switch Vss has been used. Because of this, it is obvious that larger is desirable when taking into consideration read latency and noise margin; nevertheless, the maximum value cannot be higher than this because of the limitations imposed by the area. A issue with the construction of the switch Vss is connected to the second important parameter, which is denoted by the numeral N. Therefore, it is not practical to install the switch on a cell-by-cell basis since the area overhead is more than twenty percent. Because of this, a group of cells that are close together ought to share it.

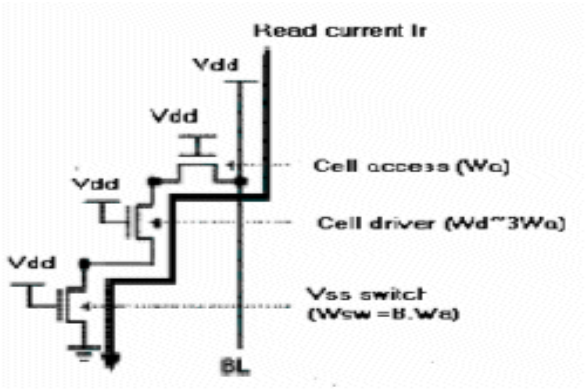


**Fig 1. Verify the seven-transistor cell's current trajectory**

There are three components in each row that are responsible for the area penalty in this case. There is a common source line that connects each cell to the switch, in addition to the switch and the SLC signal line. Furthermore, there is a common source line. Making its value equal to the bit width, which is its maximum, is the approach that does this in the fastest and simplest way possible. For the reason that will be discussed further below, however, such a configuration cannot be implemented in the actual world. A representation of the read current path for the shared switch structure can be seen in Figure 5. As the read current travels through each cell in the course of read cycles, the maximum current that may be carried over the common source line can potentially exceed N amperes. (IR)

### B. 7T SRAM with Power Analysis Resistant

This causes the cell's current dissipation and stored data have significantly less of a connection with one another. Our suggested 7T SRAM cell employs a two-phase write operation with equalization and write phases to correct the information leakage that occurs during write operations in the 6T SRAM cell.

**An Overview of the Fundamentals**

A 7T SRAM cell is being considered; Figure 3 shows a schematic of the cell. By turning off the voltage supply of a complete memory word (VVDD), a power gate PMOS transistor (PG) prevents power loss that might be caused by short circuits during the equalisation phase of the write process. Because of this, power outages may be avoided. The addition of transistor PPC to short Q and QB improves the

original 6T SRAM design at the equalisation step. Doing so reinforces the implementation even more.

To guarantee that power is restored from the VVDD source, it is essential to assert the WL provide write access to the cell. Transferring BL to Q-7T and BLB to QB-7T are necessary steps to complete the write '1' operation. It is already configured with BL connected to VDD and BLB to GND. There is a large energy disparity between the write '1' and '0' operations in a typical 6T cell (Q-6T and QB-6T). The only time these cells' internal voltages change is when the WL is asserted. But these two procedures use quite different amounts of energy.

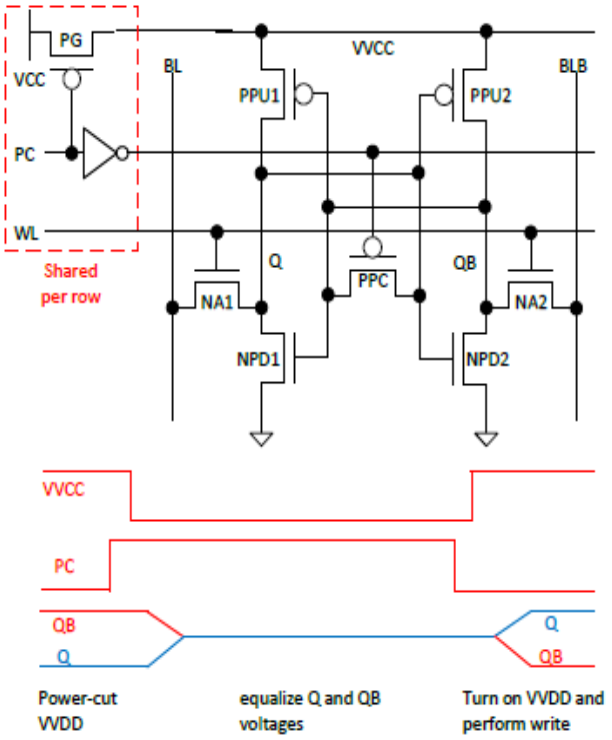


**Figure 2. A 7-transistor SRAM cell and its fundamental functioning**

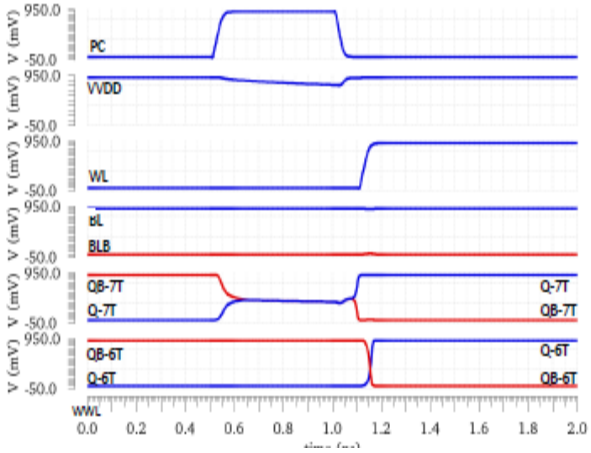


**Figure 3. Graph showing the 7T SRAM write operation's waveform**

➢ **Power Analysis**

Because 7T cells are symmetrical, the current consumption during the equalisation phase has nothing to do with the initial data input. Because VVDD is off during this phase and charge sharing equalises the voltages on Q and QB, the cell does not lose any further energy. Thus, it makes no difference whether the cell had a value of '1' or '0' earlier as far as power consumption is concerned prior to the WL assertion. Figure 5(a) shows the current dissipated from the 7T SRAM cell during the write '1' and '0' operations on a cell that had previously stored a '0'. The fact that the two-phase write operation produces waveforms that are almost identical to each other demonstrates that there is no present information leakage. Figure 5(b) shows the equivalent write energy scatter plot for the 7T SRAM cell. This resulted from a thousand MC simulations that accounted for process and instrument modifications. According to the expected results, the average energy dissipation for the write '0' operation is 2.297 fJ, while the write '1' action has an average of 2.301 fJ. The standard deviations for these two operations are 0.0345 fJ and 0.353 fJ, respectively. Compared to the distributions discovered for the 6T SRAM cell, which were equal, this leads to a far smaller discrepancy.

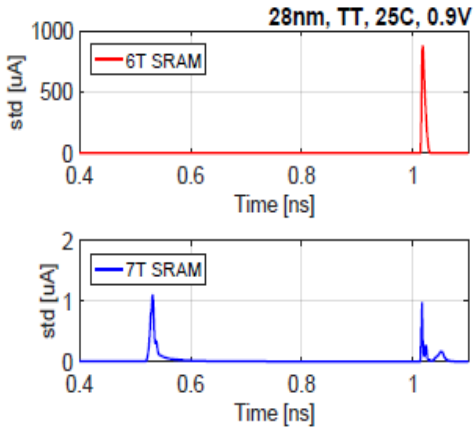


**Figure 4. Variance in current consumption during a write cycle for 6T and 7T SRAM cells with varying Hw values**

➢ ***Array Design***

To measure the performance of each cell and compare it to previous studies, we found that each cell had a 128 kilobyte array. Because all of the cells that have been compared are subject to the write-disturb issue, the array was generated using a design that was not interleaved and did not have any column-select circuitry as it was being created. There are four 32kb sub-blocks that make up the array, and each column has 1024 cells. The word size of the array is 32 bits. A technique known as fast Limited Switch Dynamic Logic (LSDL) was used in the construction of the pre-

decoders and decoders [30]. This is shown in Figure 6, which depicts the circuit implementation. There were sixty-four NOR-based pre-decoders responsible for driving the decoder-driver for each row. These pre-decoders had self-timed pulses as their outputs, and they received 10 address bits as their inputs. When contrasted with Divided-Wordline-Decoding (DWD), Hierarchical-Word-Decoding (HWD) results in a greater reduction in power consumption and a shorter amount of time required for access [31]. Because the HWD design makes use of a large number of word lines, the total capacitance per row pick route is reduced. This is the explanation for this characteristic. The gains, on the other hand, are negligible for arrays that are less than 256 kilobytes in size. Due to the low size of the array, which was 128 kilobytes, the DWD technique was used. It was decided to employ selective precharge using Block-Select (BS) to enable the precharge of bit-lines of just the available block. This was done to reduce the amount of active power that was consumed.

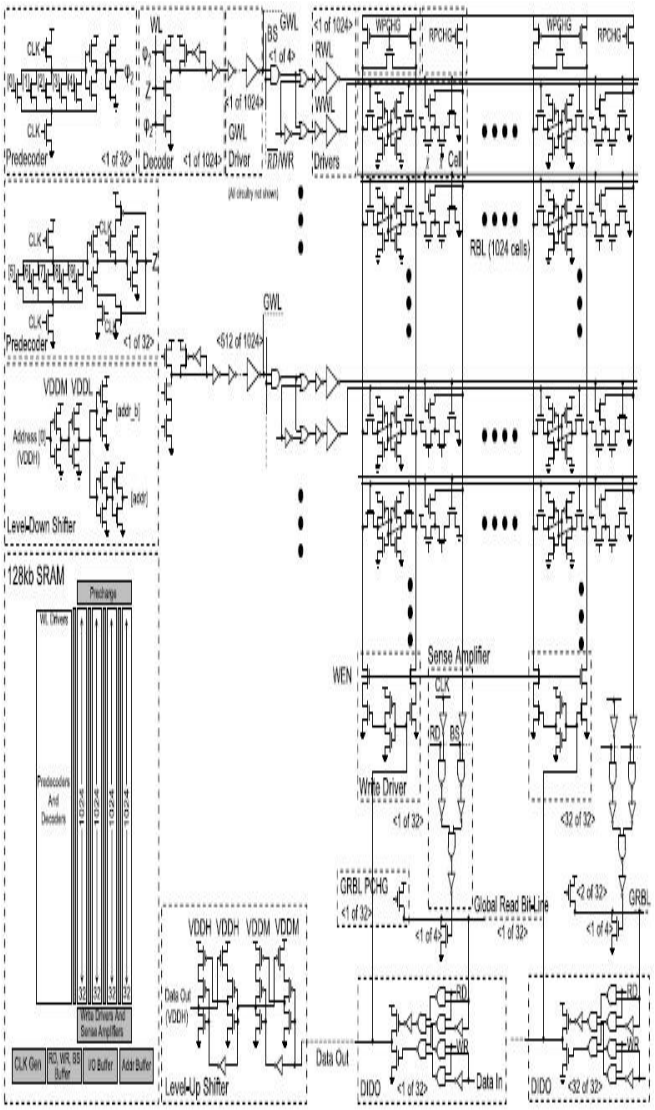


**Fig 5. The 10T-P1 cell's crucial read route includes a schematic of pre- and decoders based on Limited Switch Dynamic Logic**

Through the use of four metal layers, the VDD, GND, bit-lines, as well as the local and global word-lines, were successful in their routing. The transistor sizes of all of the cells that were measured and compared in this investigation are shown in Table I. By expanding the size of R3 nMOS, the proposed 10T-P1 cell was able to greatly increase read performance. This was made possible by the unique structure and arrangement described in the statement. Although this alteration did not result in an increase in the cell's area, it did result in a little increase in standby power.

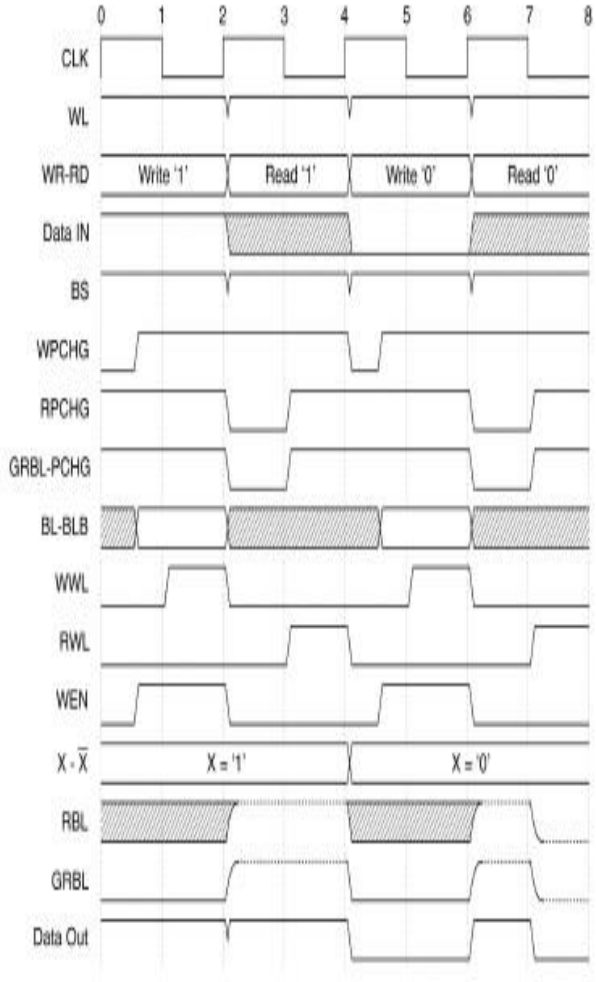


**Fig. 6. Schematic of the timing of a write-read operation in the SRAM**

Synchronizing the signals that have a positive edge is accomplished via the usage of the clock signal. When the clock signal is on the negative edge, both the local RWL and the WWL are triggered into their respective states. At the beginning of each and every operation, the WL is combined with the output of each and every predecoder to facilitate the decoding of new email addresses. First, the bit-lines are precharged at the beginning of each write operation, and then data is written onto them. This is done before the WWL controller is activated. In the same spirit, all of the global RBLs and local bit-lines of the accessible block are precharged at the midway point of the read clock cycle. With the RWL being engaged during the second half of the clock,

the RBL is given the opportunity to expand under certain conditions. Initially, the sensing amplifier will determine the voltage level of the RBL to do an evaluation of the global RBL. DIDO, which stands for "Data-In-Data-Out," is responsible for producing logical output based on the global RBL level.

- ***Read Bit-Line Swing***

The sensing amplifier is only able to produce an accurate evaluation when it is performing read operations with a read margin that is sufficiently big. In an ideal environment, this buffer would be guaranteed by the gap that exists between VDD and GND, which is a significant RBL swing. On the other hand, if all of the cells leak into the RBL or vice versa, the low logic levels may be significantly impaired, and the margin for correct detection at lower voltages may be drastically decreased. If the temperature continues to rise, the leakage current will continue to rise, which will further intensify the RBL swing's deterioration. In certain instances, the RBL swing may also be affected by the data-dependent leakage pathway that is present in the read ports of SRAM cells.

Figure 8 illustrates the effective RBL swing represented as a percentage of VDD for each cell that was investigated in this research. This swing is displayed in relation to the fact that the voltage, temperature, and data pattern varied. During the process of calculating the RBL swing, we took into consideration the three eventualities that are shown below: 1) Each and every cell in the column is associated with the value 'zero.'Every cell in the column contains the value "one" that is kept there.

In the third place, the column is composed of an equal number of twos and zeros. As can be shown in Figure 8, the effective RBL swing of the 10T-C cell is the lowest of all the cells that were investigated, and it varies significantly depending on the data pattern. It is a data-independent leakage channel in the read port of the 10T-K cell that is responsible for the RBL swing that occurs in the cell. It is also possible to see a data-dependent RBL swing in the 10T-P cell, but this swing is less varied. When compared to the 10T-C cell, the effective RBL swing of the recommended 10T-P1 cell is far less reliant on the data pattern. In spite of the fact that it is reliant on the data, the goal is to achieve high performance and near- or super-threshold functioning, where RBL swing is not a worry. All of the cells, including the 10T-P2 and the 10T-P3, exhibit a data-independent RBL swing; however, the 10T-P2 cell exhibits the most significant RBL swing of the lot.

- ***Standby Leakage Power***

Ideally, the absolute power of the cell should be as low as is practically possible throughout the board, regardless of the temperature or voltage. Consequently, Figure 9 presents a detailed examination of the average standby leakage power per cell, together with changes in voltage, temperature, and data pattern. One of the three situations that are taken into consideration while calculating standby power is the following: 1) in every cell of the array, the value "zero" is recorded. "One" is stored in each and every cell of the array.There is no difference in the distribution of "one" and "zero" (3).

Over a broad spectrum of voltages and temperatures, Figure 9 demonstrates that the cells that were proposed consume the least amount of leakage power in comparison to the cells that were used in prior experiments. Furthermore, the worst-case leakage power is created by an equal distribution of 'zero' and 'one' data for 10T-C, 10T-P, 10T-P1, and 10T-P2 cells. This is the outcome of the worst-case scenario. In most cases, the 10T-K and 10T-P3 normally display the highest leakage power when they are kept in the "zero" state. Despite this, there is a large variety of supply voltages and temperatures that diverge strongly from this trend. In spite of the fact that it is the cell that consumes the least amount of power in the near and sub-threshold regions, the 10T-P2 cell experiences a surge in its power consumption when the gate tunneling leakage current flows more quickly at higher voltages during the process. After having been lower than the 10T-C cell in the super-threshold zone, the power consumption of the 10T-P3 cell rises in the sub-threshold region at 27 degrees Celsius. Even if this trend is stable at temperatures as low as -10 degrees Celsius, it is always the case that the 10T-P3 cell consumes more power than the 10T-C cell when the temperature is 80 degrees Celsius or above.

## IV CONCLUSION

To build embedded memories that are resistant to PA attacks, certain design precautions are required. These embedded memories are constructed utilizing 6T SRAM macros. There is a considerable fraction of cryptographic systems that are comprised of embedded memory, which may store confidential information. The purpose of this study is to show a novel 7T SRAM cell that makes use of a two-phase write operation to significantly reduce the correlation between the data that is written and the amount of energy that is used. This cell is constructed by adding an additional PMOS transistor to the 6T SRAM implementation that was first used. When compared to the conventional 6T SRAM cell, the 7T SRAM cell that has been proposed achieves an energy correlation that is over one thousand times lower. Furthermore, the proposed 7T SRAM cell beats earlier PA resistant SRAM bits in terms of energy dissipation (-39%-53% lower) and write latency (19%-38% lower) by using a voltage equalization mechanism during the pre-charge phase of the write operation. This allows the 7T SRAM cell to achieve superior performance in both of these areas.

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