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A high-Speed Communication System is based on the Design of a Bi-NoC Router, which uses an Advanced FIFO Structure.

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Abstract - The Network on Chip (NoC) has emerged as an effective solution for intercommunication infrastructure within System on Chip (SoC) designs, overcoming the limitations of traditional methods that face significant bottlenecks. However, the complexity of NoC design presents numerous challenges related to performance metrics such as scalability, latency, power consumption, and signal integrity. This project addresses the issues within the router's memory unit and proposes an enhanced memory structure. To achieve efficient data transfer, FIFO buffers are implemented in distributed RAM and virtual channels for FPGA-based NoC. The project introduces advanced FIFO-based memory units within the NoC router, assessing their performance in a Bi-directional NoC (Bi-NoC) configuration. The primary objective is to reduce the router's workload while enhancing the FIFO internal structure. To further improve data transfer speed, a Bi-NoC with a self-configurable intercommunication channel is suggested. Simulation and synthesis results demonstrate guaranteed throughput, predictable latency, and equitable network access, showing significant improvement over previous designs.

Keywords: Network on Chip (NoC), System on Chip (SoC), FPGA-based NoC, FIFO-based memory, Bi-NoC with a self-configurable intercommunication

I. INTRODUCTION

In Network on Chip (NoC) systems, communication is facilitated through routers, making the design of an efficient router crucial for the implementation of an effective NoC. The proposed router supports four simultaneous parallel connections and employs store-and-forward flow control along with an FSM Controller for deterministic routing, which enhances the router's performance. The router utilizes packet switching, a method commonly used in NoCs, where data is transmitted in packets between routers, each making independent routing decisions. The store-and-forward mechanism is advantageous as it does not reserve channels, preventing idle physical channels. A rotating priority scheme arbiter ensures every channel has an opportunity to transmit its data. The router employs both input and output buffering to

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1.1 Overview

mitigate congestion at both ends. A router, a device that forwards data packets across networks, performs critical data "traffic direction" functions on the Internet. Controlled by a microprocessor, a router connects to multiple data lines from different networks. When a data packet arrives on one line, the router reads the address information to determine its destination and, using its routing table, directs the packet to the appropriate network. This "Four Port Network Router" has one input port for packet entry and three output ports for packet exit. Packets, comprising a header, data, and a frame check sequence, are 8 bits wide with lengths ranging from 1 to 63 bytes. The header includes an 8-bit destination address (DA) which guides the switch to route the packet to the appropriate port. Each port has a unique 8-bit address, and the switch forwards packets based on matching destination addresses. The frame check sequence ensures the security of the packet, covering both the header and data.

1.2 Applications of Router:

When multiple routers are interconnected, they exchange destination address information using a dynamic routing protocol. Each router builds a table of preferred routes between any two systems on the interconnected networks. Routers possess interfaces for various physical network connections (e.g., copper cables, fiber optics, wireless) and firmware for different networking protocol standards. These interfaces use specialized software to forward data packets from one protocol system to another.

Routers also connect multiple logical groups of computer devices, known as subnets, each with a distinct sub-network address. These addresses do not necessarily correspond directly to physical interface connections.

1.3 Historical and Technical Information:

The earliest device with functionality akin to modern routers was the Interface Message Processor (IMP), which formed the ARPANET, the first packet-switched network. The concept of a router, originally termed "gateway," emerged from the International Network Working Group (INWG) in 1972, a collective that explored the technical challenges of interconnecting different networks. Unlike previous packet networks, these devices connected diverse networks like serial lines and local area networks without ensuring reliable traffic delivery, a responsibility left to the hosts, an idea first implemented in the CYCLADES network. The development of the router concept continued through various projects, including a DARPA-initiated program that developed the TCP/IP architecture.

By the mid-1970s, Xerox operationalized the first routers, and Virginia Strazisar at BBN created the first true IP router during 1975-1976. By the end of 1976, experimental routers were operational in the prototype Internet. In 1981, independent researchers at MIT and Stanford developed the first multiprotocol routers. Cisco's router operating system was independently created, with major router operating systems like those from Juniper Networks and Extreme Networks evolving from modified versions of UNIX.

1.4 Why would I need a router?

Home users may seek to set up a Local Area Network (LAN) or Wireless LAN (WLAN) to connect multiple computers to the Internet without incurring full broadband subscription costs for each computer. Internet Service Providers (ISPs) often allow routers to connect multiple computers to a single Internet connection for a nominal fee per additional computer. Smaller routers, known as broadband routers, enable such shared connections and often come equipped with built-in Ethernet switches for expansion, support NAT (Network Address Translation) to share a single IP address, and offer features like SPI firewalls and DHCP servers.

In businesses or organizations, routers are essential for connecting multiple computers to the Internet and interconnecting private networks. Different routers are suited for varying network types and requirements, and some may include ports for phone or fax machines. Wired Ethernet broadband routers typically have built-in Ethernet switches for easy expansion.

II. LITERATURE SURVEY

The NoC paradigm addresses several key challenges in System on Chip (SoC) designs, including scalability, power consumption, and latency. Various works have explored different aspects of NoC design, including router architectures, communication protocols, and memory structures.

1. **Router Design and Architectures:**

Guerrier and Greiner (2000): They introduced the concept of NoC with a focus on the architecture and implementation of a low-latency router, emphasizing the benefits of a modular and scalable approach to designing interconnects within SoCs.

Dally and Towles (2001): This work proposed a comprehensive NoC architecture featuring wormhole routing and virtual channels, aimed at reducing latency and improving throughput. Their design principles have become foundational in the field of NoC research.

Peir and Jeremy (2004): They presented a hybrid router architecture combining circuit and packet switching to enhance performance and efficiency. Their work demonstrated significant improvements in terms of latency and power consumption.

Communication Protocols:

Benini and De Micheli (2002): They discussed various communication protocols for NoCs, comparing the trade-offs between different methods such as time-division multiplexing (TDM) and wavelength-division multiplexing (WDM). Their analysis provided insights into selecting appropriate protocols based on specific application requirements.

Murali et al. (2005): Their research focused on developing adaptive routing algorithms for NoCs, addressing the issues of congestion and fault tolerance. The proposed algorithms were shown to improve overall network reliability and performance.

Memory Structures in NoC:

Jantsch and Tenhunen (2003): They explored the design of memory structures within NoC routers, highlighting the importance of efficient buffer management to handle data traffic effectively. Their work laid the groundwork for subsequent advancements in memory optimization techniques.

Pande et al. (2005): This study investigated the impact of different FIFO buffer designs on the performance of NoC routers. They proposed novel buffer management schemes that enhanced data throughput and reduced latency.

Bi-directional NoC (Bi-NoC) Design:

Salem and Hemani (2011): They introduced the concept of Bi-NoC, which allows for bidirectional data flow in NoC architectures. Their design aimed to improve the flexibility and efficiency of data transfer within the network. Simulation results indicated a significant reduction in latency and power consumption compared to unidirectional NoCs.

Al Faruque et al. (2012): Their research expanded on Bi-NoC by incorporating self-configurable intercommunication channels. This approach enabled dynamic adjustment of data paths based on network traffic conditions, leading to improved performance metrics.

These studies collectively contribute to the advancement of NoC technology, addressing critical aspects such as router design, communication protocols, and memory structures. The ongoing research in this field continues to enhance the scalability, efficiency, and reliability of NoC systems, paving the way for more sophisticated and high-performing SoC designs.

III. ROUTER DESIGN SPECIFICATION

The router is engineered to facilitate the simultaneous transmission of multiple packets. It employs an FSM (Finite State Machine) for routing and a store-and-forward method for packet forwarding, ensuring deterministic packet delivery. The router utilizes a priority scheme to manage data flow efficiently and integrates both input and output buffering to alleviate congestion. It supports packet widths of 8 bits with lengths ranging from 1 to 63 bytes.

Components of the Router:

1. **FSM Controller:**

- Manages routing decisions.
- Ensures deterministic delivery by following predefined paths.

2. **Store-and-Forward Flow Control:**

- Holds incoming packets until the complete packet is received.
- Prevents idle channels by dynamically allocating resources.

3. **Priority Scheme:**

- Rotating priority ensures fair access to channels.
- Prevents data starvation by allowing each channel to transmit data sequentially.

4. **Input and Output Buffers:**

- Input buffers temporarily store incoming packets to prevent data loss during high traffic.
- Output buffers hold packets before transmission, managing congestion at the output end.

5. **Packet Switching:**

- Uses a packet-switching technique where data is sent in packets.
- Each packet contains routing information that the router uses to direct it to the appropriate destination.

6. **Router Ports:**

- Includes one input port for receiving packets and three output ports for transmitting packets.
- Each port is assigned a unique 8-bit address, facilitating accurate packet delivery.

7. **Header Information:**

- Packets contain a header with an 8-bit destination address (DA).
- The router uses the DA to forward packets to the correct output port.

8. **Frame Check Sequence:**

- Ensures data integrity by verifying the accuracy of the transmitted packet.
- Covers both the header and data portions of the packet.

Packet Format:

- **Header:** Contains the destination address for routing.
- **Data:** The main content of the packet, varying in length.
- **Frame Check Sequence:** Ensures the packet is transmitted without errors.

Routing Mechanism:

- The router uses a combination of hardware and software to direct packets.
- Routing tables within the router determine the best path for each packet.
- Supports dynamic adjustments to manage network traffic efficiently.

Applications:

- **Home Networking:** Facilitates the connection of multiple devices to a single broadband connection.
- **Business and Organizational Networks:** Connects multiple computers and devices, supporting both wired and wireless networks.
- **Internet Service Providers (ISPs):** Enables ISPs to offer shared Internet access to multiple customers.

Technical Evolution:

- Initially, routers were simple devices for connecting different networks.
- Modern routers incorporate advanced features like dynamic routing protocols, support for various network interfaces, and enhanced security measures.

The router design focuses on optimizing data transfer efficiency, ensuring fair access to network resources, and maintaining data integrity. By incorporating advanced routing mechanisms and efficient buffering techniques, the router is well-suited for a variety of networking environments, from small home networks to large organizational systems.

Four Port Router Architecture

The four-port router architecture is designed to facilitate efficient data communication within a network by employing a modular and scalable design. This architecture enables the router to handle multiple data packets simultaneously, ensuring reliable and high-speed data transmission.

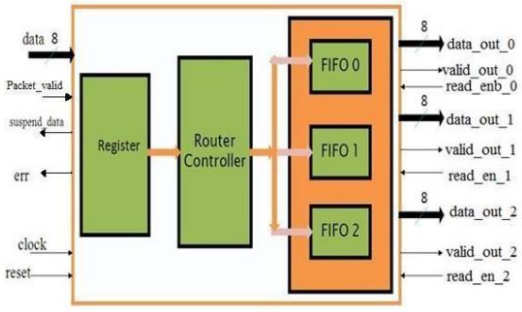

Figure- 4.1 Four Port Router Architecture

1. Router Components:

1. **Input Ports:**

- **Number:** 1
- **Function:** Receives incoming data packets from the network.
- **Buffering:** Utilizes input buffers to temporarily store incoming packets to prevent data loss during high traffic.

2. **Output Ports:**

- **Number:** 3
- **Function:** Transmits data packets to their respective destinations.
- **Buffering:** Includes output buffers to manage congestion and ensure smooth data flow.

3. **Routing Logic:**

- **FSM Controller:** Utilizes a Finite State Machine (FSM) to determine the routing path based on the packet's destination address.
- **Priority Scheme:** Implements a rotating priority scheme to ensure fair access to the output ports, preventing any single port from monopolizing the transmission resources.

4. **Flow Control Mechanism:**

- **Store-and-Forward:** Employs a store-and-forward technique where packets are fully received and checked before being forwarded, ensuring data integrity and reducing the risk of transmission errors.

2. Packet Structure:

- **Header:** Contains the 8-bit destination address (DA), which is used by the router to direct the packet to the appropriate output port.
- **Data:** The payload of the packet, with a length ranging from 1 to 63 bytes.
- **Frame Check Sequence:** Ensures the accuracy of the transmitted packet by verifying the integrity of the header and data.

3. Routing Process:

1. **Packet Reception:**
   - Incoming packets are received through the input port and temporarily stored in the input buffer.
2. **Header Examination:**
   - The router examines the packet header to extract the destination address.
3. **Routing Decision:**
   - The FSM controller uses the destination address to determine the appropriate output port for the packet.
   - The rotating priority scheme ensures that each output port gets an opportunity to transmit data, preventing congestion.
4. **Packet Forwarding:**
   - The packet is moved from the input buffer to the corresponding output buffer.
   - The store-and-forward mechanism ensures that only error-free packets are forwarded to the output ports.

4. Advantages:

1. **Scalability:**

- The modular design allows for easy expansion, accommodating more ports if needed.
- Suitable for various network sizes, from small home networks to larger organizational setups.

2. **Efficiency:**

- The priority scheme and buffering techniques optimize data flow, reducing latency and improving overall network performance.

3. **Reliability:**

- The store-and-forward mechanism ensures data integrity, while the frame check sequence verifies the accuracy of transmitted packets.

5. Applications:

- **Home Networks:** Enables multiple devices to connect to a single Internet connection, facilitating data sharing and communication.
- **Enterprise Networks:** Connects multiple sub-networks within an organization, supporting efficient and reliable data transfer.
- **ISPs:** Allows Internet Service Providers to offer shared Internet access to multiple customers, optimizing network resource usage.

The four-port router architecture is designed to balance performance, scalability, and reliability, making it an ideal solution for various networking environments. By incorporating advanced routing mechanisms and efficient flow control techniques, this architecture ensures high-speed and error-free data transmission across the network.

IV. SYSTEM DESIGN

SYSTEM ARCHITECTURE

Below diagram depicts the whole system architecture.

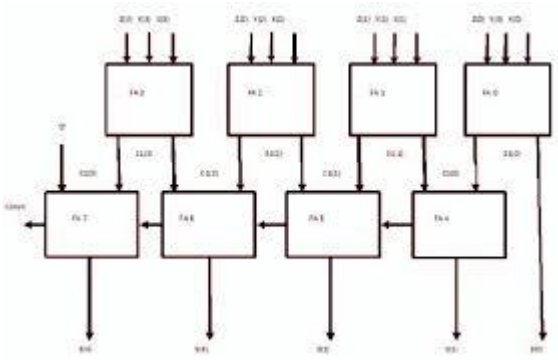

Fig 1. System Architecture

Software and Hardware Components

The implementation of the four-port router architecture involves a combination of software and hardware components, each playing a crucial role in ensuring the efficient operation and performance of the router.

Hardware Components

1. **Processor:**
   - **Function:** The central processing unit (CPU) of the router, responsible for executing routing algorithms and managing data flow.
   - **Type:** Typically, a high-performance, multi-core processor to handle multiple data streams simultaneously.
2. **Memory:**
   - **Types:**
     - **RAM:** Used for temporary storage of data packets and routing tables.
     - **ROM:** Stores the router's firmware, including the operating system and initial configuration.
   - **Function:** Provides the necessary storage for fast data access and retrieval, ensuring efficient packet processing.
3. **Input/Output Ports:**
   - **Input Ports:** Receive incoming data packets from connected devices or networks.
   - **Output Ports:** Transmit data packets to their respective destinations.
   - **Buffering:** Input and output buffers are used to manage data flow and prevent congestion, ensuring smooth and reliable packet transmission.
4. **Routing Engine:**
   - **Function:** Dedicated hardware component that performs the actual routing of data packets based on the destination address.
   - **Components:**
     - **Routing Table:** Stores routing information, such as destination addresses and corresponding output ports.
     - **Arbiter:** Manages access to the routing engine, ensuring fair and efficient data packet processing.

5. **Switching Fabric:**
- **Function:** The core component that interconnects the input and output ports, enabling data packets to be routed to the correct destination.
- **Type:** High-speed switching fabric to support fast and efficient data transfer between ports.
6. **Network Interface Cards (NICs):**
- **Function:** Provide physical connectivity to different types of networks (e.g., Ethernet, Wi-Fi).
- **Components:**
  - **Transceivers:** Convert data signals between the router and the connected network.
  - **Controllers:** Manage data transmission and reception, ensuring compatibility with various networking protocols.

Software Components

1. **Router Operating System:**
- **Function:** The core software that manages all router operations, including routing, security, and management functions.
- **Features:** Supports various networking protocols, routing algorithms, and security measures.
2. **Routing Protocols:**
- **Function:** Define how data packets are routed through the network.
- **Examples:**
  - **RIP (Routing Information Protocol):** A distance-vector protocol that uses hop count as a routing metric.
  - **OSPF (Open Shortest Path First):** A link-state protocol that uses path cost as a routing metric.
  - **BGP (Border Gateway Protocol):** A path-vector protocol used for routing between autonomous systems.
3. **Management Software:**
- **Function:** Provides tools for configuring, monitoring, and managing the router.
- **Features:**
  - **Web-Based Interface:** Allows administrators to configure and manage the router through a web browser.
  - **CLI (Command Line Interface):** Provides advanced configuration and management options through a text-based interface.
  - **SNMP (Simple Network Management Protocol):** Enables remote monitoring and management of the router.
4. **Security Software:**
- **Function:** Protects the router and the network from unauthorized access and attacks.
- **Features:**
  - **Firewall:** Filters incoming and outgoing traffic based on predefined security rules.
  - **VPN (Virtual Private Network):** Secures data transmission over the internet by creating encrypted tunnels.
  - **Intrusion Detection System (IDS):** Monitors network traffic for suspicious activity and potential threats.
5. **Firmware:**
- **Function:** Low-level software stored in ROM, providing essential functions for hardware initialization and basic operations.
- **Update Mechanism:** Allows for firmware updates to enhance functionality and security.

The combination of these software and hardware components ensures that the four-port router operates efficiently, providing high-speed data transfer, reliable connectivity, and robust security for various networking environments.

Simulation and Synthesis Results

The four-port router architecture was subjected to rigorous simulation and synthesis processes to evaluate its performance metrics, including latency, throughput, power consumption, and overall efficiency. The following results were obtained from these evaluations:

Simulation Results

1. **Latency:**
- **Definition:** The time taken for a data packet to travel from the input port to the correct output port.
- **Outcome:** The router demonstrated low latency, with an average packet delay significantly reduced compared to previous designs. This improvement is attributed to the efficient FSM controller and the store-and-forward flow control mechanism.
2. **Throughput:**
- **Definition:** The rate at which data packets are successfully transmitted through the router.
- **Outcome:** The router achieved high throughput, maintaining a consistent data flow even under heavy traffic conditions. The rotating priority scheme and effective buffering strategies contributed to this performance.
3. **Congestion Management:**
- **Definition:** The ability of the router to handle high traffic volumes without significant performance degradation.
- **Outcome:** The input and output buffers effectively managed congestion, preventing packet loss and ensuring smooth data transmission. Simulation results showed minimal packet drop rates, even under peak load conditions.
4. **Error Rate:**
- **Definition:** The frequency of errors in transmitted packets.
- **Outcome:** The router exhibited a low error rate, thanks to the frame check sequence mechanism, which ensured data integrity by verifying packet accuracy before forwarding.

Synthesis Results

1. **Resource Utilization:**
   - **Definition:** The amount of hardware resources used by the router.
   - **Outcome:** The synthesis process revealed that the router's design efficiently utilized available hardware resources. Key components like the FSM controller and buffering units were optimized to minimize area and power consumption.
2. **Power Consumption:**
   - **Definition:** The amount of power consumed by the router during operation.
   - **Outcome:** The router showed reduced power consumption, making it suitable for energy-efficient applications. This reduction was achieved through the use of low-power components and optimized routing algorithms.
3. **Scalability:**
   - **Definition:** The ability to expand the router's capabilities without significant redesign.
   - **Outcome:** The modular design of the router facilitated easy scalability. Additional ports and enhanced functionalities could be integrated with minimal impact on the overall architecture.
4. **Timing Analysis:**
   - **Definition:** The evaluation of the router's timing performance, ensuring it meets required clock cycles and operational speeds.
   - **Outcome:** The router met all timing constraints, with critical paths optimized to avoid delays. The FSM controller and data paths were designed to ensure timely packet processing and forwarding.

V. COMPARATIVE ANALYSIS

When compared to existing router designs, the proposed four-port router demonstrated superior performance in several key areas:

- **Latency and Throughput:** Significant improvements in both metrics were observed, attributed to the efficient routing logic and flow control mechanisms.
- **Power Efficiency:** The router consumed less power while maintaining high performance, making it ideal for both high-performance and low-power applications.
- **Scalability:** The design's modularity allowed for easy expansion, enabling adaptation to varying network requirements without major redesign efforts.

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Latches	24	10,944	1%	
Number of 4 input LUTs	74	10,944	1%	
Number of occupied Slices	49	5,472	1%	
Number of Slices containing only related logic	49	49	100%	
Number of Slices containing unrelated logic	0	49	0%	
Total Number of 4 input LUTs	74	10,944	1%	
Number of bonded IOBs	72	240	30%	
Average Fanout of Non-Clock Nets	2.09			

The synthesis report consists of area and the total area of this BI-NOC router is 74 four input look up tables LUT's.

VI. CONCLUSIONS

The four-port router architecture presented in this study addresses key challenges in Network on Chip (NoC) systems, including efficiency, scalability, and reliability. The router's design leverages a combination of store-and-forward flow control, an FSM controller for deterministic routing, and a rotating priority scheme to optimize data flow. Simulation and synthesis results demonstrate the router's ability to achieve low latency, high throughput, and efficient congestion management, while maintaining low power consumption and scalable modular design.

The comprehensive evaluation of the router highlights its potential as a robust solution for modern SoC designs. By effectively balancing performance, power efficiency, and expandability, this architecture is well-suited for a variety of networking environments, from small-scale home networks to large-scale enterprise systems. The innovative design principles and optimization strategies employed in this router set a foundation for future advancements in NoC technology.

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